Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2016**

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|  |  | **Semester :** | **2016-17 ODD** |
| **Code :** | **14CS2005** | **Duration :** | **3hrs** |
| **Sub. Name :** | **COMPUTER ARCHITECTURE** | **Max. marks :** | **100** |

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| Q. No | Questions | | | | Course outcome | Marks |
| **PART-A (40X1=40 MULTIPLE CHOICE QUESTIONS)** | | | | | | |
| 1. | How many opcodes are possible in a 16 bit instruction format with 4 bits allotted for opcode? | | | | CO 1 |  |
|  | a.16 | b.8 | c.32 | d.64 |  | (1) |
| 2. | Which of the following primary memory requires frequent refreshments to retain the data? | | | | CO 1 |  |
|  | a.Static RAM | b.Dynamic RAM | c.ROM | d.EEPROM |  | (1) |
| 3. | In interrupt driven I/O \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ is interrupting the CPU after completing the I/O operation. | | | | CO 1 |  |
|  | a.Memory module | b.Control unit | c.I/O module | d.Processor |  | (1) |
| 4. | Name the addressing modes which are not referring the memory for operands. | | | | CO 2 |  |
|  | 1. Register, Register indirect | b. Register, Immediate | c. Direct, Register | d. Base Register, Register |  | (1) |
| 5. | Which one of the following CPU registers holds the address of the instruction to be executed next? | | | | CO 1 |  |
|  | a.MBR | b.AC | c.IR | d.PC |  | (1) |
| 6. | The CPU nearly delays its operation for one memory cycle, to allow direct memory I/O transfer. This process is called\_\_\_\_\_\_\_\_\_\_\_\_. | | | | CO 1 |  |
|  | a.Cycle waiting | b.Cycle stalin | c.Cycle interrupting | d.Cycle executing |  | (1) |
| 7. | No of bits of K in the hamming code of an M bit data is satisfying which of the following condition? | | | | CO 2 |  |
|  | a. 2K - 1> M+K | b. 2K- 1> M+K | c. 2K - 1> M+K | d. 2K+1> M+K |  | (1) |
| 8. | DMA stands for\_\_\_\_\_\_\_\_\_\_. | | | | CO 2 |  |
|  | a. Direct Memory Address | b. Direct Memory Access | c. Direct Main Address | d. Device Memory Access |  | (1) |
| 9. | In one address instruction format the default location of the any one of the operands is \_\_\_\_. | | | | CO 1 |  |
|  | a. Accumulator | b.Stack pointer | c.Program counter | d.Instruction register |  | (1) |
| 10. | To extend the connectivity of the processor bus we use \_\_\_\_\_\_ . | | | | CO 1 |  |
|  | a. PCI bus | b. SCSI Bus | c. Controllers | d. Multiple Bus |  | (1) |
| 11. | Group of wires carrying and exchanging data between main memory, CPU and control unit is called.\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. | | | | CO 1 |  |
|  | a. System Bus | b. Data Bus | c. Control Bus | d.Address Bus |  | (1) |
| 12. | When an input electrical signal A=10100 is applied to a NOT gate, its output signal is | | | | CO 2 |  |
|  | a. 01011 | b. 10001 | c. 00101 | d.10101 |  | (1) |
| 13. | The classification of BUS’s into synchronous andasynchronous is based on | | | | CO 2 |  |
|  | a.The devices connected to them | b.The type of data transfer | c.The Timing of data transfers | d.None of the above |  | (1) |
| 14. | \_\_\_\_\_\_ BUS arbitration approach uses the involvement of the processor | | | | CO 2 |  |
|  | a. Centralized | b. Distributed | c. Random | d. All of these |  | (1) |
| 15. | How many times a processor with 32 bit data bus want to access the main memory to fetch a 64 bit instruction? | | | | CO 2 |  |
|  | a. 1 | b. 2 | c. 3 | d. 4 |  | (1) |
| 16. | A 0 in the sign bit represents a \_\_\_\_\_\_\_\_\_\_\_\_\_ and a 1 in the sign bit represents a \_\_\_\_\_\_\_\_\_\_\_\_: | | | | CO 1 |  |
|  | a. Positive number | b. Negative number | c.  Both | d.      None of these |  | (1) |
| 17. | Which algorithm is a multiplication algorithm which multiplies two signed binary numbers in 2’s complement notation: | | | | CO 2 |  |
|  | a. Usual multiplication | b. Booth’s multiplication | c. Both | d.  None of these |  | (1) |
| 18. | Which number is said to be normalized if the more significant position of the mantissa contains a non zero digit: | | | | CO 1 |  |
|  | a. Binary point number | b. Mantissa point number | c. Floating point number | d.      None of these |  | (1) |
| 19. | A machine language instruction format consists of | | | | CO 1 |  |
|  | a) Operand field | b) Operation code field | c) Operation code field & operand field | d) none of the mentioned |  | (1) |
| 20. | The instructions like MOV or ADD are called as \_\_\_\_\_\_ . | | | | CO 2 |  |
|  | a) OP-Code | b) Operators | c) Commands | d) None of the above |  | (1) |

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| 21. | Which method/s of representation of numbers occupies large amount of memory than others ? | | | | | CO 2 |  |
|  | a) Sign-magnitude | b) 1’s compliment | c) 2’s compliment | | d) Both a and b |  | (1) |
| 22. | When we perform subtraction on -7 and 1 the answer in 2’s compliment form is \_\_\_\_\_ . | | | | | CO 2 |  |
|  | a) 1010 | b) 1110 | c) 0110 | | d) 1000 |  | (1) |
| 23. | The most efficient method followed by computers to multiply two unsigned numbers is \_\_\_\_\_\_\_ . | | | | | CO 2 |  |
|  | a) Booth algorithm | b) Bit pair recording of multipliers | c) Restoring algorithm | | d) Non restoring algorithm |  | (1) |
| 24. | Which addressing mode execute its instructions within CPU without the necessity of reference memory for operands? | | | | | CO 2 |  |
|  | a. Implied Mode | b. Immediate Mode | c. Direct Mode | | d. Register Mode |  | (1) |
| 25. | In case of, Zero-address instruction method the operands are stored in \_\_\_\_\_ . | | | | | CO 2 |  |
|  | a) Registers | b) Accumulators | c) Push down stack | | d) Cache |  | (1) |
| 26. | Cache memory works on the principle of | | | | | CO 1 |  |
|  | a.Locality of data | b.Locality of reference | c.Locality of memory | | d.Temporal reference |  | (1) |
| 27. | What is the type of instruction that has any one of the operands act as source and destination operands? | | | | | CO 2 |  |
|  | a.Zero address | b.One address | c.Two address | | d.Three address |  | (1) |
| 28. | What is the two’s complement representation of +2? | | | | | CO 2 |  |
|  | a.0010 | b.0011 | c.1101 | | d.1100 |  | (1) |
| 29. | Assume a six stage pipeline. Each stage takes one millisecond to finish. If there are 9 instructions in the pipeline, calculate the time duration in milliseconds required to finish 9 instructions. | | | | | CO 2 |  |
|  | a.54 | b.58 | c.14 | | d.16 |  | (1) |
| 30. | There are multiple instructions in the pipeline enter into the execution stage when there is one ALU. What type of hazard is this? | | | | | CO 2 |  |
|  | a.Structural hazard | b.Data hazard | c.Control hazard | | d.Branch hazard |  | (1) |
| 31. | The number of cycles the pipeline is stalled due to wrong branch decision is called\_\_\_\_\_. | | | | | CO 2 |  |
|  | a.Control penalty | b.Decision penalty | c.Hazard penalty | | d.Branch penalty |  | (1) |
| 32. | What is the purpose of the mode field in any instruction? | | | | | CO 2 |  |
|  | a. Specifies the number of operands | b. Specifies the opcode | c. Specifies the addressing mode | | d. Specifies the access mode |  | (1) |
| 33. | The signal sent by any 8237A DMA controller to the processor to request the system bus is called\_\_\_. | | | | | CO 1 |  |
|  | a. DREQ | b. DACK | c. HREQ | | d. HLDA |  | (1) |
| 34. | Which of the following I/O mechanisms suitable for multiple word data transfers? | | | | | CO 1 |  |
|  | a.Interrupt Driven | b.Programmed I/O | c.DMA | | d.Multiword |  | (1) |
| 35. | To increase the performance of an instruction pipeline which two of the following are to be done?   1. Increase the number of stages 2. Decrease the number of stages 3. Make the duration of each stage equal 4. Make the duration of each stage unequal | | | | | CO 2 |  |
|  | a.i only | b.ii only | c.i and iii | | d.i and iv |  | (1) |
| 36. | Which of the following is the simplest but inflexible scheme of control unit? | | | | | CO 2 |  |
|  | a.Hardwired | b.Microprogrammed | | c.Wilks | d.Booth |  | (1) |
| 37. | When an instruction is writing into a register after the previous instruction writing the same register is called | | | | | CO 2 |  |
|  | a. RAW | b.WAW | c.WAR | | d.RAR |  | (1) |
| 38. | The portion of the memory that stores a collection of microinstructions of a microprogram is called\_\_\_\_\_\_. | | | | | CO 2 |  |
|  | a.ROM | b.RAM | c.Control memory | | d.Stack |  | (1) |
| 39. | The register that stores the address of the next microinstruction to be executed is | | | | | CO 2 |  |
|  | a.Memory Address Register | b.Control Address Register | c.Program Counter | | d.Memory Buffer Register |  | (1) |
| 40. | Which of the following is not the role of control unit? | | | | | CO 2 |  |
|  | a.Sequencing | b.Execution | c.Data transfer | | d.Coordination |  | (1) |

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| **PART B(8 X 5 = 40 MARKS) (ANSWER ANY EIGHT)** | | | |
| 41. | Write short notes on associative mapping. | CO 1 | (5) |
| 42. | Define Interrupt. For MUL A,C instruction, draw the instruction cycle state diagram with interrupts and explain the steps involved. | CO 1 | (5) |
| 43. | Differentiate SRAM and DRAM. | CO 1 | (5) |
| 44. | Describe the DMA mechanism with a suitable architecture diagram. | CO 1 | (5) |
| 45. | Evaluate unsigned binary multiplication algorithm with 5×4. | CO 2 | (5) |
| 46. | Differentiate logical shift and arithmetic shift with suitable examples. | CO 1 | (5) |
| 47. | Write short notes on the different types of data processed by a computer. | CO 2 | (5) |
| 48. | Consider that the following two instructions are executed in a sequential fashion.  ADD EAX, EBX /\* EAX = EAX + EBX  SUB ECX, EAX /\* ECX = ECX – EAX  Identify and explain the type of hazard suffered from by the SUB instruction and propose a solution to overcome the same. | CO 2 | (5) |
| 49. | Draw the instruction cycle state diagram with interrupt cycle. | CO 1 | (5) |
| 50. | Brief on the micro operations of indirect cycle with pseudocode. | CO 2 | (5) |
| **PART C( 2 X 10 = 20 MARKS) (ANSWER ANY TWO)** | | | |
| 51. | Consider an 8 bit data 00111001 to be stored into memory. Assume that the third data bit is suffering from error and changing from 0 to 1. Compute the hamming code and syndrome word for this data and prove that the third data bit is affected by error. | CO 1 | (10) |
| 52. | Illustrate various addressing modes with suitable diagrams. | CO 2 | (10) |
| 53. | Discuss the different pipeline hazards with necessary examples and explain the methods of resolving the data hazards. | CO 2 | (10) |

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